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HAYNES AND BOONE, LLP			EXAMINER	
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Dallas, TX 75202			ART UNIT	PAPER NUMBER
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The time period for reply, if any, is set in the attached communication.



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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/714,304  
Filing Date: November 14, 2003  
Appellant(s): CHEN ET AL.

Steven T. Mc Donald  
For Appellant

**MAILED**  
NOV 09 2007  
**GROUP 2800**

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed March 23, 2006 appealing from the Office action mailed August 23, 2005.

**(1) Real Party of Interest**

A statement identifying the real party of interest is contained in the brief.

**(2) Related Appeals and Interferences**

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

**(3) Status of Claims**

The statement of the status of the claims contained in the brief is correct.

**(4) Status of Amendments**

The statement of the status of the amendment after final is correct.

**(5) Summary of Claimed Subject Matter**

The summary of the invention contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appealed**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) References of Record**

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

US 2004/0166669	Saito	08-2004
US 2003/0054629	Kawai et al.	03-2003

### **(9) Grounds of Rejection**

The following grounds of rejection are applicable to the appealed claims:

Claims 1, 4-8, 10-14, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito (US2004/0166669) in view of Kawai et al. (US 2003/0054629).

With respect to claim 1, Saito discloses providing a structure having an overlying exposed conductive layer (1) formed there over; forming a dielectric layer (2) over the conductive layer Page 1, Paragraph [0027]; etching the dielectric layer using a via opening process to form an initial via (3) exposing a portion of the conductive layer (See Fig. 1B and Page 2, Paragraph [0028]); forming a protective film portion (4) over at least the exposed portion of the conductive layer (Page 2, Paragraph [0029]), the protective film portion being comprised of the elements C and H; patterning the dielectric layer (2) to reduce the initial via to a reduced via and to form a trench opening (6) substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening (See Figs. 1E, 1F and Page 2, Paragraphs [0030], [0031] and [0032]).

Saito does not disclose forming an anti-reflective coating layer over the dielectric layer and etching the anti-reflective layer to form an initial via; and then patterning the anti-reflective layer to reduce the initial via.

Kawai et al. disclose providing a structure having a conductive layer (2) (Page 3, Paragraph [0047]); forming a dielectric layer (3) over the conductive layer (Page 3, Paragraph [0048]); forming an anti-reflective coating layer (4) over the dielectric layer (Page 3, Paragraph [0049]); etching the anti-reflective layer (4) and the dielectric layer using a via opening process to form an initial via (6) (See Fig. 1A and Page 3, Paragraph [0050]); forming a protective film portion (17) (See Fig. 1B and Page 3, Paragraph [0053]); patterning the anti-reflective locating layer and the dielectric layer (3) to reduce the initial via to a reduced via and to form a trench opening (10) substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening (See Fig. 1C and Page 3, Paragraph [0054]).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Saito and Kawai et al. to enable the anti-reflective coating layer formation step of Kawai et al. to be performed in the process of Saito because it will improve the dimension accuracy of the initial via (6) (Page 3, Paragraph [0051] of Kawai et al.

Re claim 4, Kawai et al. disclose wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

Re claim 5, Kawai et al. disclose wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

Re claim 6, Kawai et al. disclose wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

Re claim 12, Kawai et al. disclose including the step of forming an etch stop/liner layer (16) over the exposed conductive layer.

Re claim 13, Kawai et al. disclose disclose including the step of forming an etch stop/liner layer (16) over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 200 to 1500 Å, which overlaps the recited thickness of claim 13 (50 to 2000 Å) and being comprised of the elements Si and C such as SiC.

Re claim 14, Kawai et al. disclose disclose including the step of forming an etch stop/liner layer (16) over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 200 to 1500 Å, which overlaps the recited thickness of claim 13 (100 to 1000 Å) and being comprised of the elements Si and C such as SiC.

Re claim 16, Saito discloses wherein a via plug is formed within the initial via before formation of the trench opening (See Fig. 1B).

Re claim 18, Saito discloses wherein the formation of trench opening utilizes a patterned photoresist-masking layer (5) as a mask.

Re claim 19, Saito discloses wherein the formation of trench opening utilizes a patterned photoresist-masking layer (5) as a mask.

Re claims 7, 8, 10 and 11, One of ordinary skill in the art would have been led to the recited thicknesses, temperature, pressure time and plasma power through routine experimentation to achieve a desired rate of annealing, device dimension, device associated characteristics and device density on the finished wafer. See MPEP 2144.05. In addition, the selection of thicknesses, temperature, pressure time and

plasma power, it's obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species of result effective variables. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill or art) and In re Aller, 105 USPQ 233 (CCPA 1995) (selection of optimum ranges within prior art general conditions is obvious).

Note that the specification contains no disclosure of either the critical nature of the claimed thicknesses, temperature, pressure time and plasma power or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen thicknesses, temperature, pressure time and plasma power or upon another variable recited in a claim, the Applicant must show that the chosen thicknesses, temperature, pressure time and plasma power are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 2, 3, 9 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15, 20-22 and 43-50 are allowed.

#### **(10) Response to Argument**

Appellant argues that layer 4 of Saito cannot be interpreted as being a "protective film" but instead is a "via fill". However, layer 4 of Saito can be interpreted as a protective film because prevents a Cu interconnection from being damaged by trench formation etching. Furthermore, this is merely labelling, Saito's polymeric member 4 can be labeled as a "protective film".

Appellant argues that the subject application makes clear that the characterization of the protective film is made in conventional sense of the term "film" including the film formation mechanism CVD. However, it is noted that the features upon which applicant relies (i.e., CVD process) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant argues that the definition of a "film" by the Merriam Webster dictionary is:

1. a thin skin or membranous covering
2. a thin covering or coating



3. an exceedingly thin layer

Thus, the dictionary definitions of the subject term indicates, interpretation of the conductive polymeric member as a film is inconsistent with the plain meaning given to the term "film" as the conductive polymeric member vial fill described by Saito is not shown or otherwise characterized in any manner consistent with the plain meaning.

However, the definition of "film" as described above, as being a "thin membranous covering or a thin covering or coating" encompasses the instant claim as the polymeric member 4 of Saito could be a "thin coating". The term "thin" is a relative term, which renders the claim indefinite. The term "thin" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably appraised of the scope of the invention.

**(11) Related Proceeding(s) Appendix**

The appeal brief filed March 23, 2006 does not include an evidence appendix or a related proceedings appendix. The examiner assumes that there is no evidence submitted by the appellant and no related proceedings since there are no related proceedings listed in the related appeals and interferences section and it is assumed that the appellant meant to include both appendixes with a statement of "NONE."

See MPEP 1205.02=1205.03.

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

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For the above reasons, it is requested that the honorable Board of Patent Appeals  
and Interferences sustain the rejections above.

Respectfully submitted,

Conference:



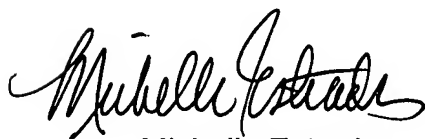
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October 29, 2007